CLAIMS:

1. Data processing device, at least comprising a master controller (1), a first functional unit (2) which includes a slave controller (20), a second functional unit (3), which functional units (2,3) share common memory means (11), the device being programmed for executing an instruction by the first functional unit (2), the execution of said instruction involving input/output operations by the first functional unit (2), wherein output data of the first functional unit (2) is processed by the second functional unit (3) during said execution and/or the input data is generated by the second functional (3) unit during said execution.

2. Data processing device according to claim 1, characterized in that the first functional unit (2) is arranged for processing instructions of a first type corresponding to operations having a relatively large latency and in that the second functional unit (3) is arranged for processing instructions of a second type corresponding to operations having a relatively small latency.

3. Data processing according to claim 1, having halt means controllable by the master controller (1) for suspending operation of the first functional unit (2).

4. A method of operating a dataprocessor device, which device comprises at least

- a master controller (1) for controlling operation of the device
- a first functional unit (2), which includes a slave controller (20), the first functional unit (2) being arranged for executing instructions of a first type corresponding to operations having a relatively long latency,
- a second functional unit (3) capable of executing instructions of a second type corresponding to operations having a relatively short latency, wherein the first functional unit (2) during execution of an instruction of the first type receives input data and provides output data, according to which method the output data is processed by the second functional unit (3) during said execution and/or the input data is generated by the second functional unit (3) during said execution.

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5. Method according to claim 4, characterized in that, the master controller (1) temporarily suspends operation of the first functional unit (2) during execution of instructions of the first type.

6. A method for compiling a program into a sequence of instructions for operating a processing device according to claim 1, according to which method

- a model is composed which is representative of the input/output operations involved in the execution of an instructions by a first functional unit (2),
- on the basis of this model instructions for the one or more second functional units (3) are scheduled for providing input data for the first functional unit (2) when it is executing an instruction in which said input data is used and/or for retrieving output data from the first functional unit (2) when it is executing an instruction in which said output data is computed.

7. A method according to claim 6, characterised in that the model is a signal flow graph

Restrict claims 6+7
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